8

Comparisons of BJT and MOSFET

8.1 NMOS and NPN Transistors

- Circuit symbols and physical structures
  - NMOS has symmetric structure for drain and source.
  - NPN has asymmetric structure for collector and emitter.
- Current
  - NMOS: current flows from drain to source.
  - NPN: current flows from collector to emitter.
- Voltage
  - NMOS: $v_D > v_S$, $v_G > v_S$.
  - NPN: $v_B > v_E$, $v_C > v_E$. 

![NMOS Circuit Symbol](image1.png)

![NPN Circuit Symbol](image2.png)

![NMOS Physical Structure](image3.png)

![NPN Physical Structure](image4.png)
8.1.1 NMOS Triode v.s. NPN Saturation

- NMOS Triode $i_D - v_{DS}$ v.s. NPN Saturation $i_C - v_{CE}$
• NMOS
  – The two terminals \textit{drain} and \textit{source} act as a \textit{resistor} controlled by \((v_{GS} - V_t)\).

• NPN
  – The two terminals \textit{collector} and \textit{emitter} act as a \textit{resistor} controlled by \(I_B\) (or \(v_{BE}\)).

<table>
<thead>
<tr>
<th>Bias</th>
<th>NMOS Triode</th>
<th>NPN Saturation</th>
</tr>
</thead>
<tbody>
<tr>
<td>(v_{GS}) &gt; (V_t), (v_{DS}) &lt; (v_{GS} - V_t)</td>
<td>(v_{BE}) &gt; 0.5, (v_{CE}) &lt; (v_{BE} - 0.4 \approx 0.3)</td>
<td></td>
</tr>
</tbody>
</table>

\[ i - v \]
\[ i_D = k_n \frac{W}{L} \left[ (v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2 \right] \]
\[ r_o \]
\[ r_{DS} \approx k_n \frac{W}{L} (v_{GS} - V_t)^{-1} \approx \frac{v_{DS}}{i_D} \]

\[ r_{CE} \approx 1/10 \beta_f I_B \]

• Equivalent \textit{large signal model}

\[ i_{DS} = \frac{1}{2} k_n \frac{W}{L} (v_{GS} - V_t)^2 \]
\[ i_C \approx I_S e^{v_{BE}/V_T} - \frac{I_S e^{v_{BE}/V_T}}{\alpha_r} \]

\[ r_{CE} \approx 1/10 \beta_f I_B \]

8.1.2 NMOS Saturation v.s. NPN Forward Active

• NMOS
  – The two terminals \textit{drain} and \textit{source} act as a \textit{current source} controlled by \((v_{GS} - V_t)\).

• NPN
  – The two terminals \textit{collector} and \textit{emitter} act as a \textit{current source} controlled by \(I_B\) (or \(v_{BE}\)).

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\[ i_D = \frac{1}{2} k_n \frac{W}{L} (v_{GS} - V_t)^2 \]
\[ i_C \approx I_S e^{v_{BE}/V_T} = \beta_i_B \]

\[ r_o \]
\[ r_{DS} = \frac{V_A}{I_D} \]
\[ r_{CE} \approx \frac{V_A}{I_C} \]

• Equivalent \textit{large signal model}
8.1.3 NMOS Cut-off v.s. NPN Cut-off

- NMOS
  - $V_{GS} < V_t$.

- NPN
  - $V_{BE} < 0.5$, $V_{BC} < 0.4$.

8.2 PMOS and PNP Transistors

- Circuit symbols and physical structures
  - PMOS has symmetric structure for drain and source.
  - PNP has asymmetric structure for collector and emitter.

- Current
  - PMOS: current flows from source to drain.
  - PNP: current flows from emitter to collector.

- Voltage
  - PMOS: $v_D < v_S$, $v_G < v_S$.
  - PNP: $v_B < v_E$, $v_C < v_E$.

- $i_D - v_{DS}$ (common source) v.s. $i_C - v_{CE}$ (common emitter)
8.2.1 PMOS Triode v.s. PNP Saturation

- NMOS Triode $i_D - v_{SD}$ v.s. NPN Saturation $i_C - v_{EC}$

- PMOS
  - The two terminals source and drain acts as a resistor controlled by $v_{SG} - |V_t|$. 

PMOS $[v_{DS} \rightarrow v_{SD}, (v_{GS} - V_i) \rightarrow (v_{SG} - |V_t|), -V_A \rightarrow -|V_A|]$ 

PNP $[v_{CE} \rightarrow v_{EC}, v_{BE} \rightarrow v_{EB}, -V_A \rightarrow -|V_A|]$
• NPN
  
  - The two terminals emitter and collector acts as a resistor controlled by $I_B$.

<table>
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<th>PNP Saturation</th>
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<tbody>
<tr>
<td>Bias</td>
<td></td>
</tr>
<tr>
<td>$v_{SG} &gt;</td>
<td>V_i</td>
</tr>
<tr>
<td>$i - v$</td>
<td></td>
</tr>
<tr>
<td>$i_D = k_p^W \frac{W}{L}(v_{SG} -</td>
<td>V_i</td>
</tr>
<tr>
<td>$r_o$</td>
<td></td>
</tr>
<tr>
<td>$r_{DS} \simeq k_p^W (v_{SG} -</td>
<td>V_i</td>
</tr>
</tbody>
</table>

• Equivalent large signal model

### 8.2.2 PMOS Saturation v.s. PNP Forward Active

• NMOS
  
  - The two terminals source and drain acts as a current source controlled by $v_{SG} - |V_i|$.

• PNP
  
  - The two terminals emitter and collector acts as a current source controlled by $I_B$ (or $v_{EB}$).

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<td>Bias</td>
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</tr>
<tr>
<td>$v_{SG} &gt;</td>
<td>V_i</td>
</tr>
<tr>
<td>$i - v$</td>
<td></td>
</tr>
<tr>
<td>$I_D = \frac{1}{2}k_p^W (v_{SG} -</td>
<td>V_i</td>
</tr>
<tr>
<td>Early Effect</td>
<td></td>
</tr>
<tr>
<td>$i_D = I_D(1 +</td>
<td>\lambda</td>
</tr>
<tr>
<td>$r_o$</td>
<td></td>
</tr>
<tr>
<td>$r_{DS} =</td>
<td>V_A</td>
</tr>
</tbody>
</table>

• Equivalent large signal model
8.2.3 PMOS Cut-off v.s. PNP Cut-off

- **PMOS**
  - \( V_{SG} < |V_t| \).

- **PNP**
  - \( V_{EB} < 0.5, V_{CB} < 0.4 \).